Lab Number 5 Report

Ben Simpson, Section # 001

Benjamin Bergeson, Section # 001

**Introduction**

In this lab, we will be building the receiver board for the laser tag system. This circuit amplifies the signal from the photodiode receiver so that it can be read by the Zybo Board. Using this signal, the board can then determine whether or not the player has been shot.

The basic design for the receiver board circuit involves three parts: the photodiode/resistance combination, the voltage amplification stage, and the voltage limiter. The photodiode/resistance stage converts the current generated by the photodiode into voltage using a 3.3 kΩ resistor as a voltage divider. This stage provides some of the amplification necessary to meet the requirement of a gain between 5 and 10 million V/A. The rest of the necessary gain comes from the voltage amplification stage, which uses BJTs to amplify the voltage. The final part of the circuit, the voltage limiter, ensures that the output voltage is less than 1 Vpp by clipping the signal for high currents produced by the photodiode, thus allowing the signal to be passed to the Zybo Board under a variety of input conditions.

In addition to amplifying the signal from the photodiode, the receiver filters out extraneous signals, since the guns use only a limited range of frequencies for identification when shooting. The receiver board is also designed to consume very little power since it runs off of a 9V battery. The full specifications of the receiver board are detailed below.

**Specifications**

These are the specifications for the receiver board:

* Gain: 5x106 V/A – 10x106 V/A
* Maximum output voltage: 1V
* Bandpass filter built into amplifier
  + At least second order with 10 kHz<fH<20 kHz
* Total current draw less than 1mA
* Output impedance less than 500W

**Voltage Amplifier Design**

Since the photodiode/resistor part of the receiver board circuit produces a gain of 3300 V/A, in order to obtain a total gain of between 5 and 10 million V/A, our voltage amplification stage would need to be between 1500 and 3000 V/V. We decided to use three stages of around 13 V/V gain each in order to create a total gain of about 2200 V/V in the amplification stage, which translates to a gain of 7.2x10­6 V/A in the overall receiver board. In order to achieve the necessary gain between in each of the stages, we decided that we needed a CE amplifier followed by a CC amplifier in each stage. The CE amplifier would produce most of the voltage gain while the CC amplifier would act as a buffer in order to reduce loading. This brought the total number of BJTs up to six.

Using the same formulas as lab 4 we were able to determine the values for the CE stage of the amplifier. Since the gain of a CE amplifier is approximately equal to Rc/Re, we chose that ratio to be 15. We determined that this would give us enough gain to still achieve our goal of 13 V/V even after losses due to loading between stages. We chose Rc = 150 kΩ and Re = 10 kΩ so that the power draw through the circuit would be low.

The values of R1 and R2 were selected to create a voltage divider so that the BJT is in the active regime. Since the supply voltage used in the circuit is 9 V, our original design was to center the output voltage of the CE amplifier at 4.5 V for maximum headroom in amplifying the signal. After attempting that biasing and having it not work, we realized that this was unrealistic since the 15:1 ratio between Rc and Re would push the voltage at the output node far below 4.5 V. Using LTSpice, we adjusted the values of R­1 and R2 until our desired gain was achieved.

The circuit and the resistor values for the CE stage can be seen in Figure 1.

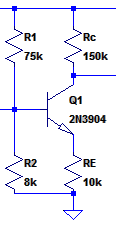


Figure 1 Initial values for the CE stage

For the CC stage, our main goal was to reduce loading between it and the CE stage. In order to do this, we made the input impedance of the CC stage much higher than the output impedance of the CE stage. The output impedance of the CE stage is Rc which we selected to be 150 kΩ, so we wanted the input impedance of the CC stage to be at least 10 times that, or 1.5 MΩ. The input impedance of our CC stage is given by the equation:

Rin = (Rπ + βRe + Rb) || R3 || R4 (Eq. 1)

R3 and R4 are the biasing resistors at the base of the BJT. We chose the values of R3 and R4 to be above 3 MΩ, which would give Rin a value of at least 1.5 MΩ provided that the summation term in the parallel resistor combination in (Eq. 1) could be ignored. We then assumed that β = 300 and chose Re of the CC stage to be 100 kΩ, making the sum at the left of (Eq. 1) a value of approximately 30 MΩ. Since this is much larger than R3 and R4, we could now ignore the term entirely in the computation as we had desired to do.

Once the CE and CC amplifiers were designed, we put them together into a single circuit and made some adjustments in LTSpice until it worked. This resulting circuit can be seen in Figure 2. Note that coupling capacitors are used between the two stages to maintain the correct bias points.

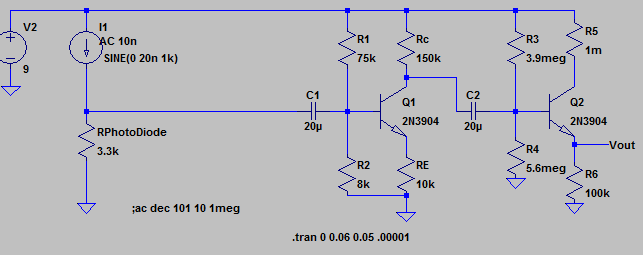


Figure 2 circuit for combination of CE and CC stages

We then duplicated the two amplifiers and added them together to create our envisioned six stage amplifier. With all six stages, the voltage amplifier should have had a total gain of around 2200 V/V, which was our goal.

**Bandpass Filtering**

Now that the voltage amplifier had the correct gain, we altered the design slightly so that it would act as a 2nd order bandpass filter as described in the specifications. We chose a lower corner frequency of 150 Hz and an upper corner frequency of 15 kHz. Using the schematic values we were able to calculate the capacitors needed to achieve our upper and lower corner frequencies.

For the lower corner frequency, we decided to adjust the value of the coupling capacitor between the 2nd CC stage and the 3rd CE stage. In order to calculate the value of the capacitor needed for the lower corner frequency, we first had to calculate the Rin of the CE BJT. The calculations for the Rin of the CE BJT and the lower corner frequency can be seen in Figures 3 and 4 respectively.

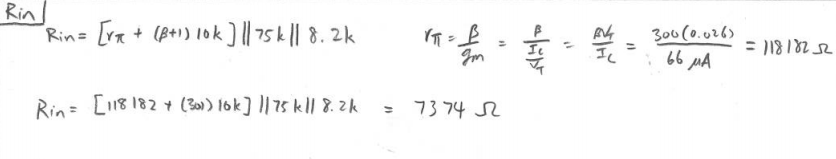


Figure 3 Calculations for Rin of the 3rd CE stage

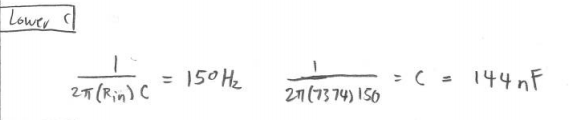


Figure 4 calculations for lower corner frequency capacitor

To create the upper corner frequency, we added a capacitor in from the node between the 3rd CE and CC stages to ground. The value of this capacitor can be determined by using the output impedance of the 3rd CE stage. The type of calculation that we used to determine the capacitor value needed to achieve our upper corner frequency can be seen in Figure 5.

(Note that the value for the output impedance of 3rd CE stage does not match its predicted value from Figure 2. This calculation was made after some circuit tuning had already taken place. To match the circuit in Figure 2, the value 120k—which is the output impedance, in ohms, of the 3rd CE stage—should be replaced with 150k. The corresponding capacitor value is 70.7 pF.)

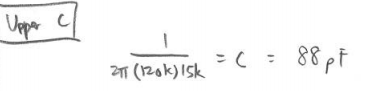


Figure 5 Sample calculation for upper corner frequency

**Voltage Limiter Design**

With the voltage amplification stage complete, we moved on to the voltage limiter. In order to limit the output voltage, we placed a diode in parallel with the output, so that the output could not get higher than the diode’s turn-on voltage. Figure 6 shows entire circuit up to this point.

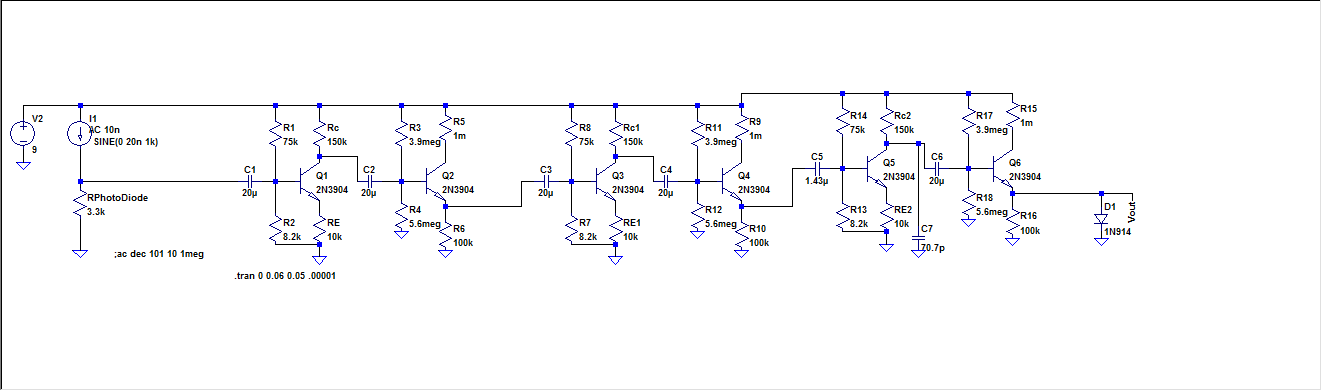


Figure 6 Full circuit diagram before tuning.

After adding the diode, we noticed that the gain had been cut drastically in our circuit simulations. We eventually determined that the diode had lowered the voltage on the emitter of the 3rd CC stage and put it into saturation. We simply adjusted the biasing on the base of that BJT, and our gain returned.

**Simulations**

After obtaining our basic design, we ran simulations and made further adjustments to the stages in order to meet the specs. The first simulation that we ran that met the gain specification can be seen in Figure 7. This yielded a gain of 5.71E6 V/A, which is within the specified 5E6 and 10E6 V/A.

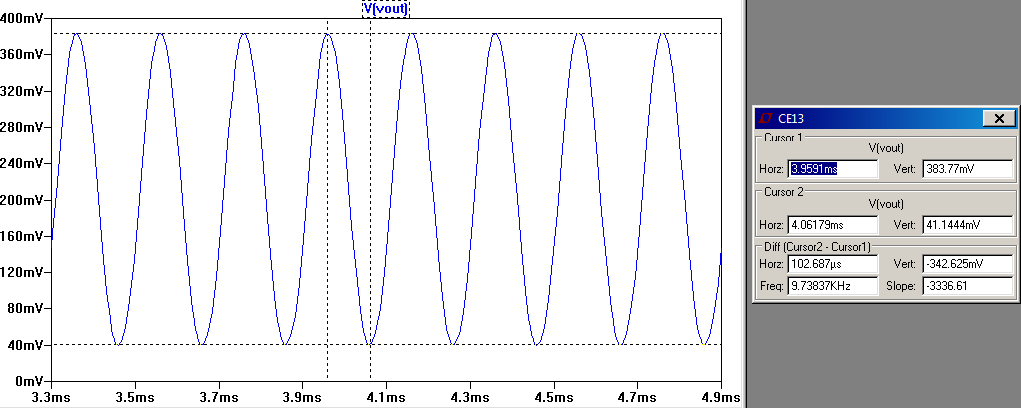


Figure 7 Gain simulation

We also ran frequency response simulations in order to determine that our voltage amplifier was performing its bandpass filtering correctly. We needed to slightly adjust our calculated capacitances in order for our corner frequencies to be where we want them to be. We ultimately adjusted the capacitance for the lower corner frequency to be 165nF and the capacitance for our upper corner frequency to be 140 pF. The simulation for the lower and upper corner frequency can be seen in Figure 8 and 9 respectively.

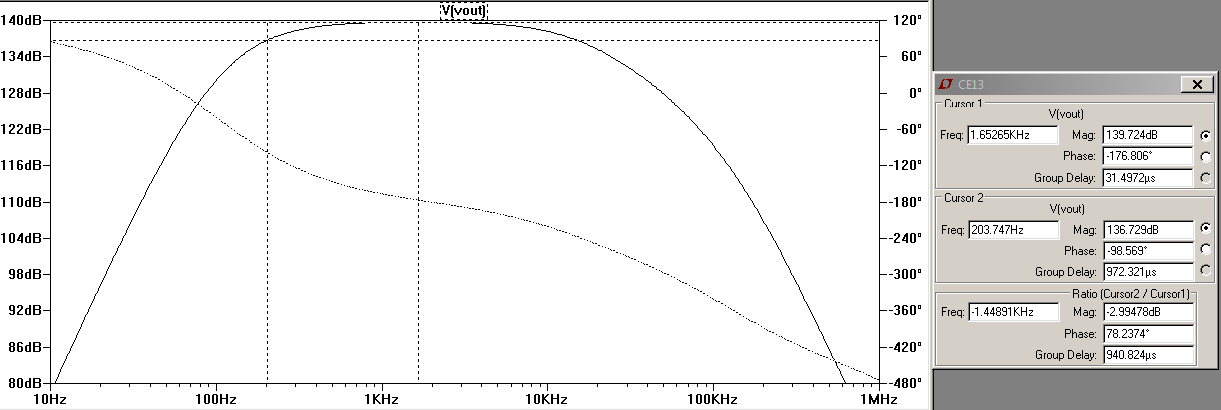


Figure 8 lower corner frequency

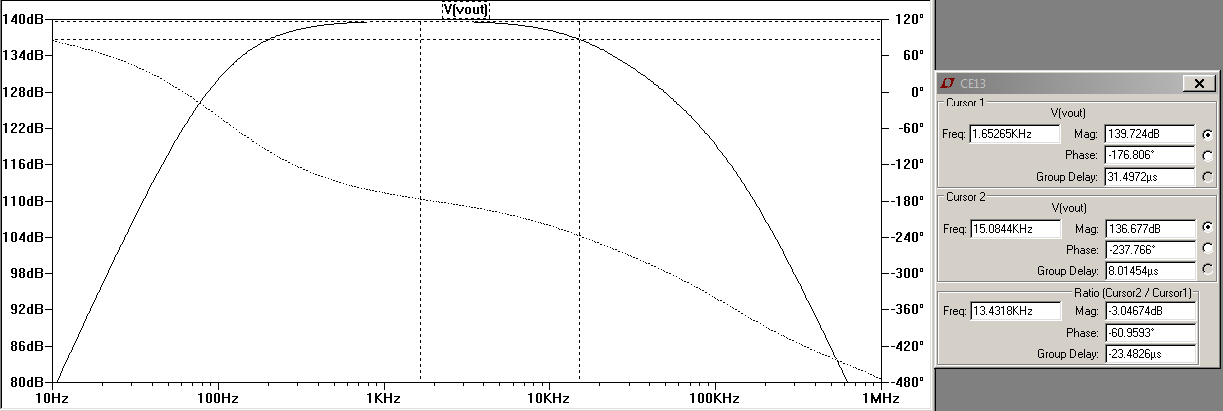


Figure 9 upper corner frequency

The next thing that we needed to run simulations on is the power consumption. In order to test the power consumption of our circuit, we hooked up a 20 nA input and then a 100 µA input to see if either one of them drew too much power from the power source. The simulations for both can be seen in Figures 10 and 11 respectively. As can be seen from the simulations, under reasonable input values, the power draw from the power source is never more than 900 µA. This is within out lab specification of 1 mA.

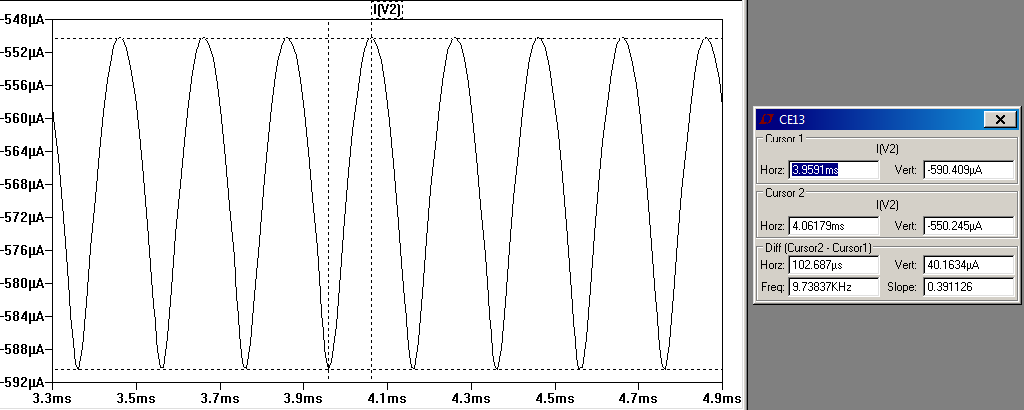


Figure 10 power consumption for a 20 nA input

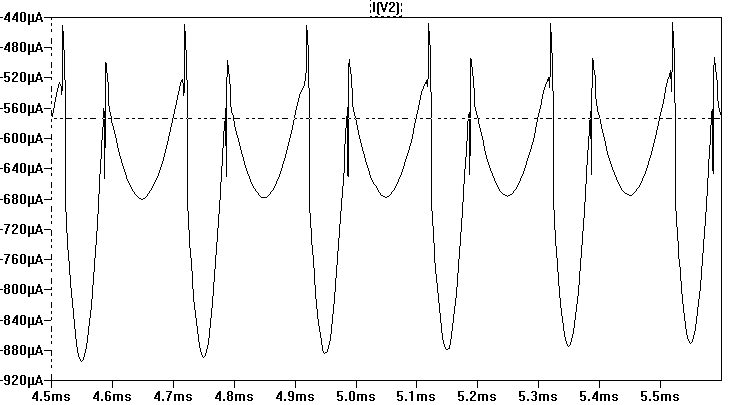


Figure 11 power consumption for a 100 µA input

The final simulation that needed to be ran for us to meet specifications is the voltage limiting portion of the circuit. We increased the input current to its maximal expected value of 100 µA and checked the output to make sure that it did not exceed 1 V. Figure 12 shows the results of this simulation, and it can be observed that the output voltage is limited to 500 mV, which is within spec.

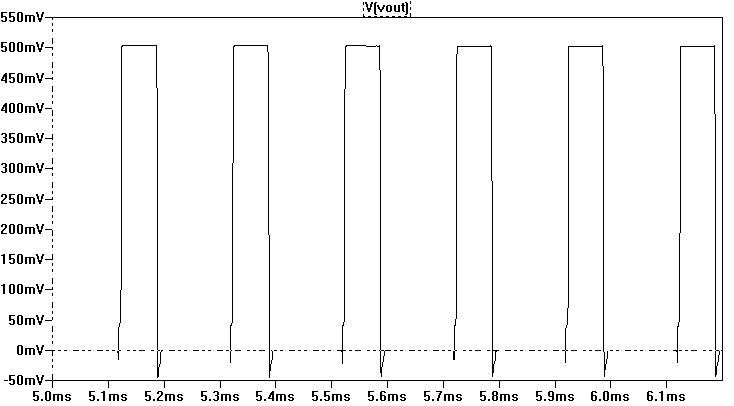


Figure 12 output voltage with voltage limiter in place

Now that our circuit met most of the specifications, we made sure that it also met the specification for output impedance. We did hand calculations on our circuit (with the value of Ic being determined by our LTSpice simulation) and made some small adjustments to the circuit until the output impedance was within spec. The final calculations for the output impedance after all adjustments were made can be seen in Figure 13. As we can see the final output impedance is 482 Ω which is less than the maximum allowed value of 500 Ω from the spec.

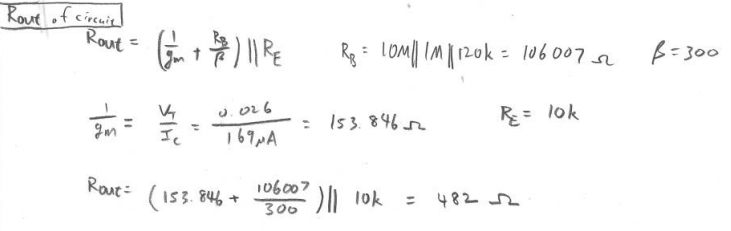


Figure 13 calculations for output impedance

**Breadboard and Testing**

Now that we have designed a circuit that works in simulations in LTSpice, we assembled it on the breadboard. After building the circuit on the breadboard, there were many things that we had to test. The first thing that we tested was the total gain of the circuit without the voltage limiter. We took the Fourier transform of the output voltage (Figure 14) and divided that by the Fourier transform of the input voltage (Figure 15.) This gave us a gain of around 280. This was way below what we were hoping for and what had been simulated.

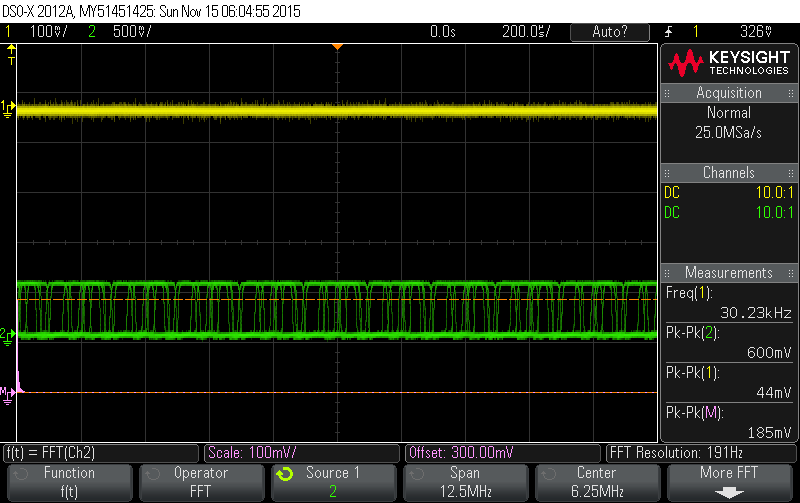


Figure 14 output across all stages without voltage limiter

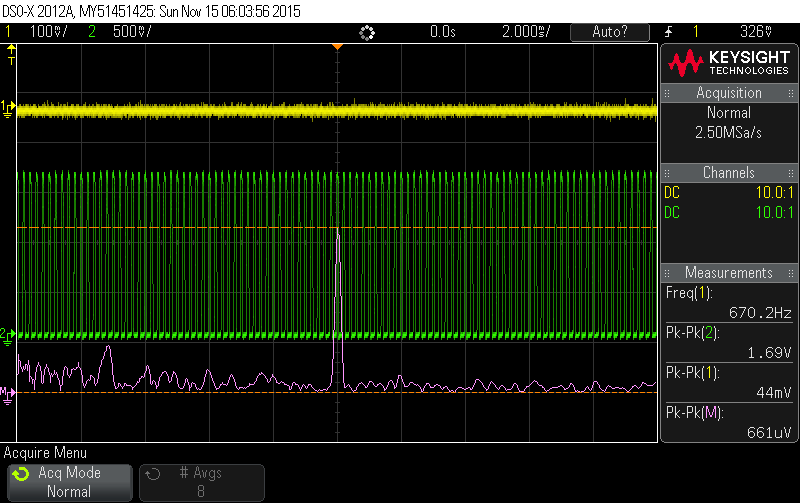


Figure 15 input voltage

We then decided to try measuring the gain across just the first two stages. We arrived at a gain of 280 after dividing the Fourier transform of the output voltage across the first two stages (Figure 16) by the input voltage (Figure 17.)



Figure 16 output across two stages

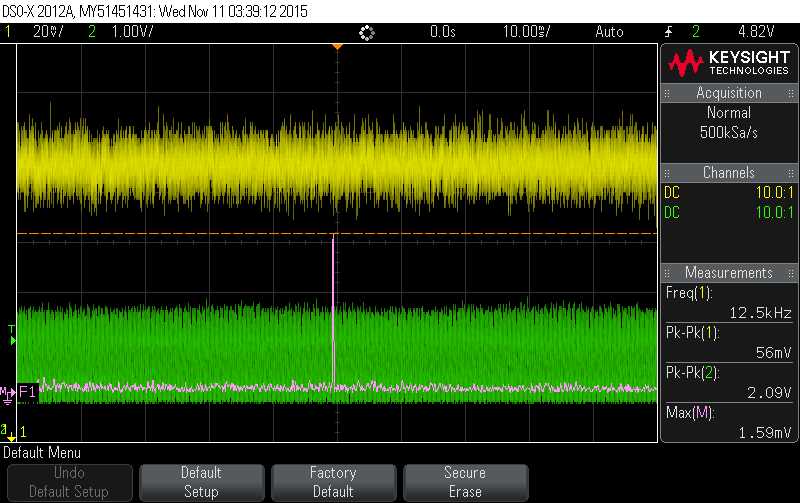


Figure 17 input voltage for just two stages

From this, we were able to discern that there was no gain across the final stage of the circuit. We also noticed that there was a lot of clipping in the output across all stages. We were then able to figure out that the last CE BJT was in saturation. Somehow the LTSpice simulation had not taken this into account. We were able to rectify this by switching out the 120 kΩ resistor between the collector of the CE BJT and the power source with a 100 kΩ resistor. Because of the change on that resistor we had to recalculate the capacitor value needed to achieve the upper corner frequency as well.

After doing so, we tested our circuit once again, this time at 2 kHz, which should have no attenuation. We measured the gain to be 8.63 by dividing the output voltage (Figure 18) by the input voltage (Figure 19.) For testing purposes, we had a 1 MΩ resistor between the function generator and the input voltage node at the beginning of the circuit, so this gain of 8.63 V/V would be equivalent to 8.63 x 106 V/A gain, which is right in between the 5 x 106 and 10 x 106 that we needed.



Figure 18 output voltage @ 2kHz

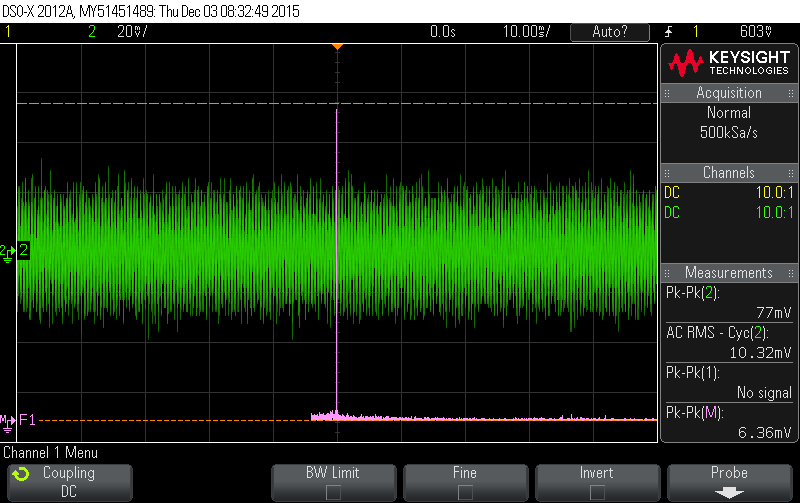


Figure 19 input voltage @ 2 kHz

Next we tested the upper and lower corner frequencies. We calculated a lower corner frequency of 170 Hz. With the oscilloscope we were able to measure a lower corner frequency of 280 Hz (Figure 20.)

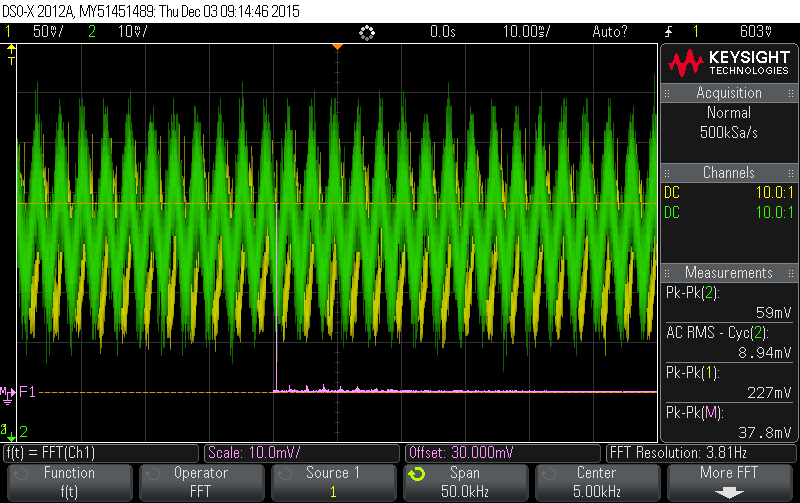


Figure 20 lower corner frequency - 280 Hz

We adjusted the upper corner frequency to be 10.9 kHz in order to filter out some output voltage spikes at around 13 kHz that we thought were caused by the fluorescent lights in the lab. Using the oscilloscope we were able to determine the actual upper corner frequency to be 10.9 kHz (Figure 21).



Figure 21 upper corner frequency - 10.9 kHz

After the tests on our corner frequencies, we measured our power consumption. Within a reasonable input voltage we saw that the maximum power consumption from the battery is around 0.66 mA.

Our final circuit design can be seen in Figure 22. The overall schematic had changed quite a bit from the original schematic shown in Figure 6. The values that changed as we fine-tuned our circuit include: the coupling capacitors between each stage, the capacitors that determine the corner frequencies, and the resistors around the final CC BJT.

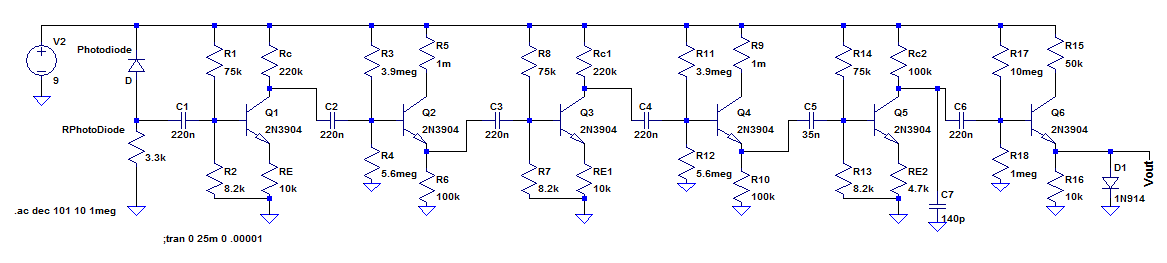


Figure 22 final schematic

**Soldering and Pass Off**

We took our breadboarded circuit and created a soldered version of it on a PCB. The only major changes between our final soldered circuit and our breadboarded one were the incorporation of a switch to turn the 9 V power supply on and off as well changing the capacitor for the lower corner frequency. After observing some low-frequency noise on the output, we raised the lower corner frequency in order to reduce it. In reality, it had little effect, and did not hinder us from passing off anyway. Our final PCB is shown in Figure 23.



Figure 23 Final PCB circuit

Our circuit passed off both of the final tests with flying colors. It had successfully met the specifications.

**Conclusion**

In this lab, we designed a circuit to amplify a signal from a photodiode so that it can be used by the Zybo board. This entailed not only amplifying the signal, but also limiting the output voltage and bandwidth as well as ensuring that the entire system does not consume too much power. Working to meet these requirements not only helped us apply our knowledge about BJT circuit topologies, but also gave us practical experience with issues related to amplifier circuits.

The final circuit was broken down into three major parts for us by the lab instructions: the photodiode/resistance combination, the voltage amplification stage, and the voltage limiter. The design of the first of these three was already given to us, so it was up to us to design the latter two.

The voltage amplification stage was the first part that we designed and was, by far, the more difficult of the two. As per the lab specifications, we needed to design a circuit that would have a gain of between 5 x 106 and 10 x 106 V/A, or between 1500 and 3000 V/V. Using the previous lab as a template, we decided that we wanted six BJT amplification stages. They would be arranged in an alternating pattern between a CE and CC topology with the CE stages amplifying the signal and the CC stages buffering the signal for the next stage. This proved to be no easy task. We did many calculations, many of which proved completely useless as we simulated and fine-tuned our circuit. After much trial and error, we were finally able to come up with a combination of CE and CC BJT topology that would yield a gain of around 13. The hope with this was that with a gain of 13 and three stages would give us around 2197.

Once we got the first stage worked out, we simply duplicated it twice and connected them together. This worked fine for us to get the gain that we needed. However, upon further testing, we realized that this was way over the specification given for power consumption. We rectified this problem by significantly increasing the resistor values between the collector of the CC BJTs and the power source. Of course once we changed those resistor values, something else would no longer be in spec. We had to go back and forth several times, adjusting resistor values as we went along, before we arrived at a circuit that worked. Having had to do this multiple times really showed us the many considerations and tradeoffs when designing a larger circuit.

Even after the simulations were all working, we still had problems when we tried to build the simulated circuit on our breadboard. The hope is that the simulations would be somewhat close to reality. However, we noticed in our circuit that something went horribly wrong between the simulation and the breadboard. We were not getting the gain that we had simulated. Instead, we got something much smaller. This was due to the fact that LTSpice had not taken into account the fact that the final CE BJT would be in saturation with the resistors that we had simulated with. After discovering this fact, we were able to use hand calculations and further simulations to adjust the value of the resistor that was putting that particular BJT into saturation to a value that would not cause it to do so.

Once we got the breadboard working and up to the specifications, we had to move everything over and solder the many components onto our board. In retrospect, perhaps we should have soldered parts of the circuit on and tested them as we went along. This would have prevented, or at least sped up the discovery and rectification, of the problem that we ran into. After testing our soldered board we noticed that we were getting very strange outputs. We discovered that this was due to a capacitor being soldered into the wrong place that turned a CE BJT into a CB BJT. It definitely helped us to have two pairs of eyes looking over everything so that we could discover this problem quicker.

Once the problems were finally ironed out, our circuit was complete. We tested it and found it to be within spec. It was able to successfully complete the TA pass offs. It made us happy and a little proud to see this circuit that we had put so much time into finally work. At the beginning of this lab, we had no idea how to design our circuit. Through some use of the design principles that we learned in class as well as a lot of tinkering, we were able to accomplish the task. From this lab, we have learned more about BJT amplifiers and the associated design principles and pitfalls than either of us ever wanted to learn, but we have also proven that we can solve complex design problems. It is this problem solving ability that makes us engineers, and it is the greatest single take-away from this lab.